```
ld.a  r30 <- [r20]
        :
        :
        :
ld.c  r30 <- [r20]
```

ALAT

#	VALID	TYPE	REG-ID	ADDRESS
n				
n-1				
n-2				
n-3				
n-4				
n-5	1	int	r30	xxyy
n-6				
n-7				
⋮				
2				
1				
0				

110 ~

FIGURE 1

```
ld.a   r30 <- [r20]
        :
        :
st   [r80] <-  r40
        :
        :
        :
ld.c   r30 <- [r20]
```

ALAT

#	VALID	TYPE	REG-ID	ADDRESS
n				
n-1				
n-2				
n-3				
n-4				
n-5	0	int	r30	xxyy
n-6				
n-7				
⋮				
2				
1				
0				

220~ 210~

FIGURE 2

```
ld.a r30 <- [r20]
   :
ld.c r30 <- [r20]
  ↓DECODE↓
ld.a r30 <- [r20]
   :
ld.con r30 <- [r20], r30
  ↓REGISTER RENAME↓
ld.a rp60 <- [rp50]
   :
ld.con rp80 <-[rp50],rp60
```

ALAT

#	VALID	TYPE	REG-ID	ADDRESS
n				
n-1				
n-2				
n-3				
n-4				
n-5				
n-6				
n-7				
⋮				
2	1	int	rp60	xxzz
1				
0				

310~

FIGURE 3

```
ld.a   r30 <- [r20]
add    r10 <- r30, r15
sub    r35 <- r30, r15
st     [r80] <- r45
chk.a  r30          (r30 destination)
```

ALAT

#	VALID	TYPE	REG-ID	ADDRESS
n				
n-1				
n-2				
n-3				
n-4	0	int	r30	xxyy
n-5				
n-6				
n-7				
⋮				
2				
1				
0				

420 410

FIGURE 4

```
ld.a r30 <- [r20]
sub r35 <- r30, r15
st [r80] <- r45
chk.a r30                    (r30 destination)
      ↓DECODE↓
ld.a r30 <- [r20]
sub r35 <- r30, r15
st [r80] <- r45
chk.a r30                    (r30 source)
   ↓REGISTER RENAME↓
ld.a rp60 <- [rp50]
sub rp65 <- rp60, rp25
st [rp85] <- rp55
chk.a rp60                   (rp60 source)
```

ALAT

#	VALID	TYPE	REG-ID	ADDRESS
n				
n-1				
n-2				
n-3				
n-4				
n-5				
n-6	0	int	rp 60	xx zz
n-7				
⋮				
2				
1				
0				

520 510

FIGURE 5

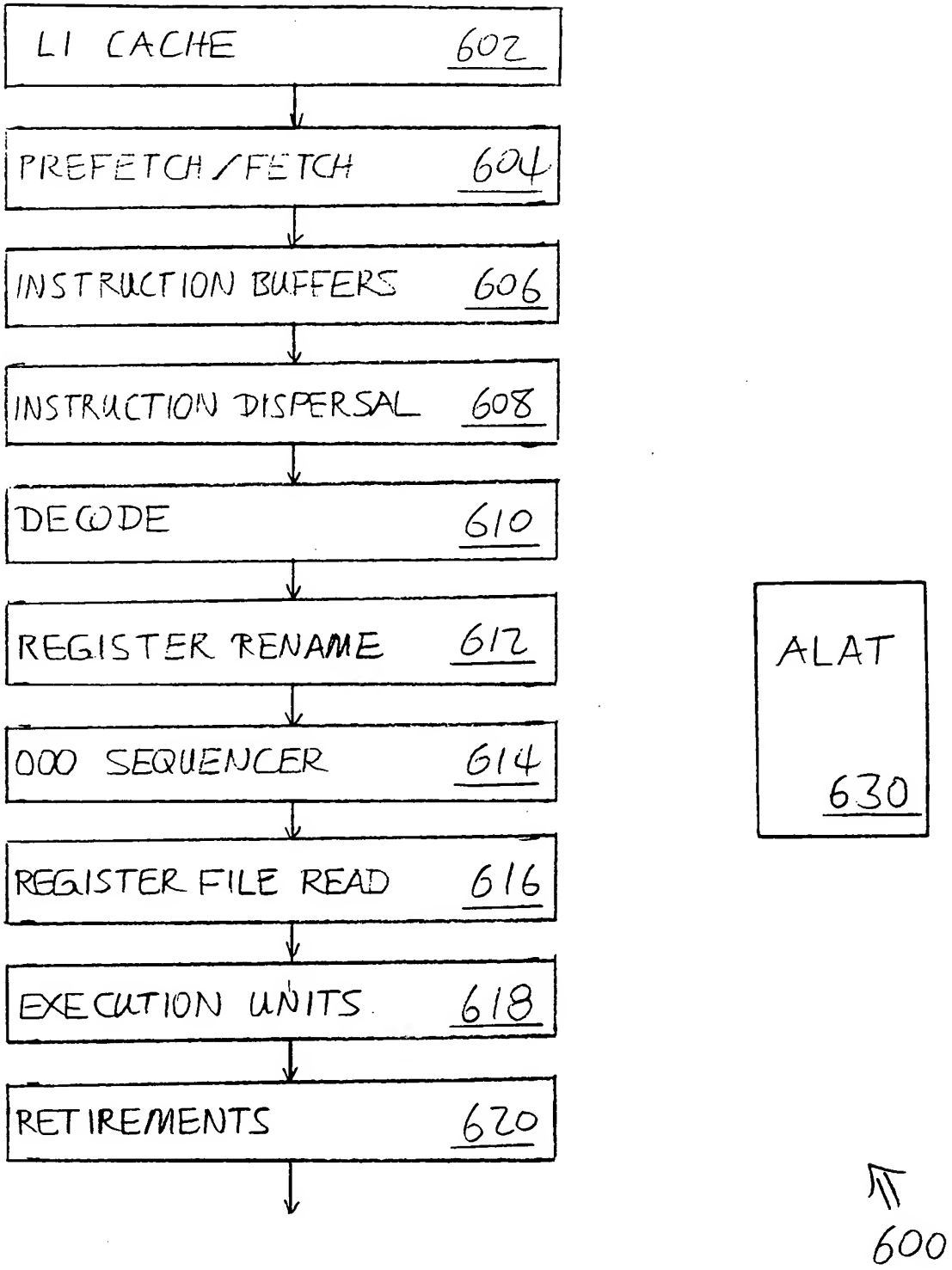
L1 CACHE 602
PREFETCH/FETCH 604
INSTRUCTION BUFFERS 606
INSTRUCTION DISPERSAL 608
DECODE 610
REGISTER RENAME 612
OOO SEQUENCER 614
REGISTER FILE READ 616
EXECUTION UNITS 618
RETIREMENTS 620
ALAT 630
600

FIGURE 6

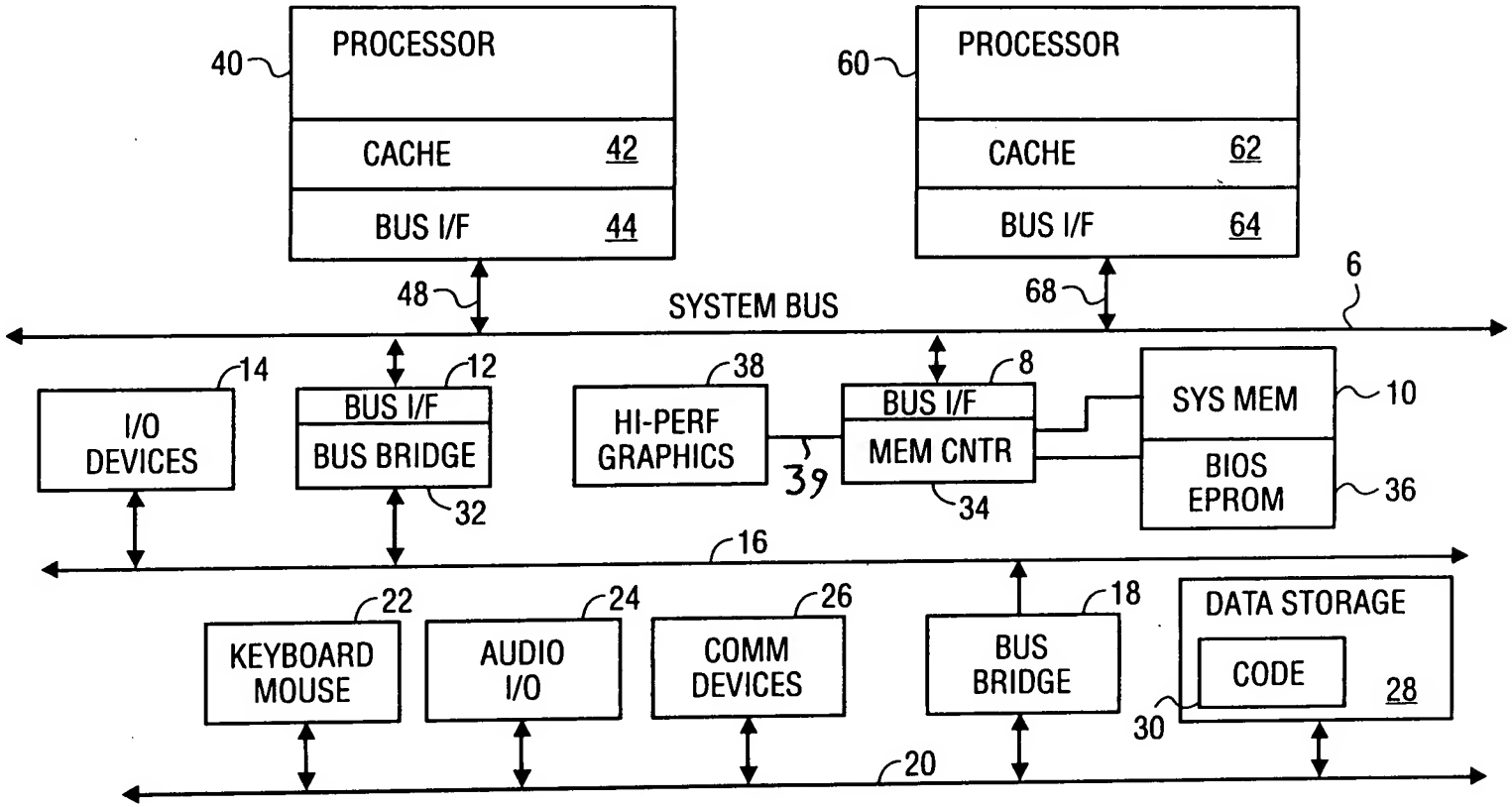
PROCESSOR
40
CACHE
42
BUS I/F
44
PROCESSOR
60
CACHE
62
BUS I/F
64
48
68
6
SYSTEM BUS
14
I/O DEVICES
12
BUS I/F
BUS BRIDGE
32
38
HI-PERF GRAPHICS
39
8
BUS I/F
MEM CNTR
34
SYS MEM
10
BIOS EPROM
36
16
22
KEYBOARD MOUSE
24
AUDIO I/O
26
COMM DEVICES
18
BUS BRIDGE
DATA STORAGE
CODE
28
30
20

FIG. 7A

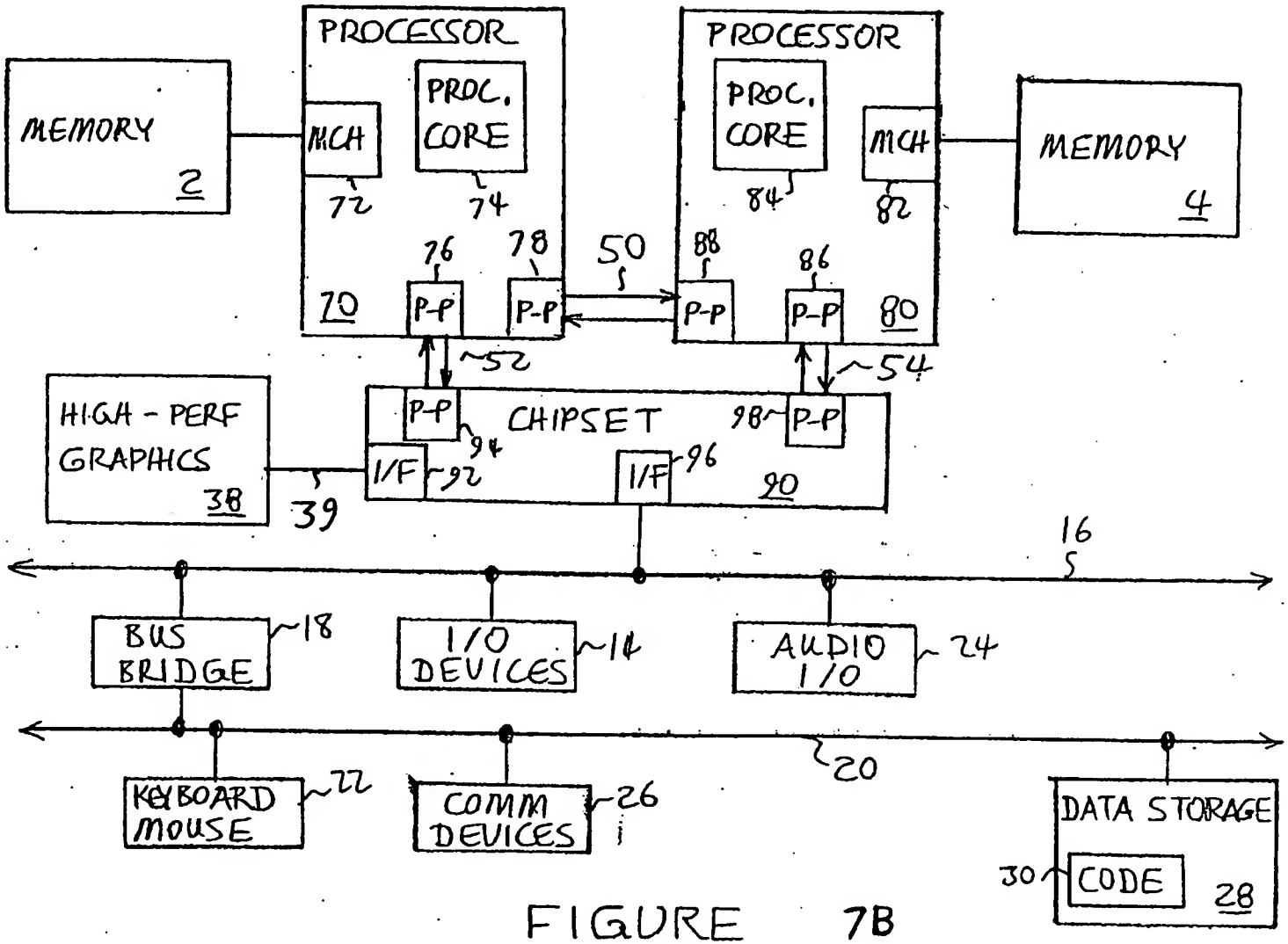
PROCESSOR
PROCESSOR
MEMORY
2
MCH
PROC. CORE
72
74
PROC. CORE
MCH
MEMORY
4
84
82
76
78
50
88
86
70
P-P
P-P
P-P
P-P
80
52
54
HIGH - PERF GRAPHICS
38
39
P-P
CHIPSET
98
P-P
94
I/F
92
I/F
96
90
16
BUS BRIDGE
18
I/O DEVICES
14
AUDIO I/O
24
20
KEYBOARD MOUSE
22
COMM DEVICES
26
DATA STORAGE
30
CODE
28

FIGURE 7B